# A Low Phase Noise LC VCO for 6GHz

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***Abstract***: *This paper is presented a cross- coupled VCO with low phase noise and low power. The VCO was simulated in 0.18µm CMOS process. The proposed VCO exhibits an operation frequency from 5.65 GHz to 7 GHz with a tuning rage of 23.89%. The simulated phase noise is -115.5 dBc/Hz at 1 MHz offset in 6.68 GHz, when VCO consumes 3.84 mw using 1.2 v supply voltage. The calculated figure of merit of this design is -186.7 dBc/Hz.*

***Keyword***: *phase noise, power, voltage controlled oscillator (VCO), tuning range.*

## 1. Introduction

Recently, the demands have increased in designing of high frequency circuits with good performance in communication circuits. Voltage-controlled oscillator is one of the most important modules of the transceivers. The most important parameter which is considered in VCO is low phase noise and power consumption. Phase noise reduction circuit is always associated with an increase in power consumption [1-3]. Therefore, The VCO phase noise and power consumption in the design will be the opposite of each other, so the design of low phase noise and low power consumption oscillation instruments will be noticeable. The topology is commonly used in the design of VCO are ring oscillator and LC- oscillator.

As shown in Fig.1, ring oscillator is composed of a number of delay steps that the output of the last stage fed back to the input. To realize oscillation, the ring must present a phase shift of 2π and have unity voltage gain at the oscillation frequency. Phase shift are performed by an inverter. Ring oscillator has two general types; a single ended ring oscillator and Differential loop Ring oscillator [4-5]. Due to ease occupy less on-chip integration area are adopted in wireless communication applications, but phase noise is high. Also, the high phase noise in the today's system is unacceptable.

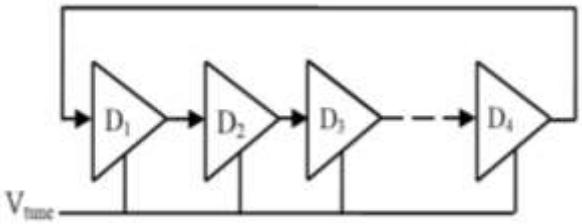


Fig. 1: Ring voltage control oscillator.

On the other hand, LC VCO achieves low phase noise and low power consumption [6]. A voltage-controlled oscillator conventional LC is shown in Fig. 2, that oscillator resonates with an inductor and capacitor. $R_C$ and $R_L$ are the parasitic resistance of the inductance and the capacitance, respectively. The negative resistance is omitted losses of tank.

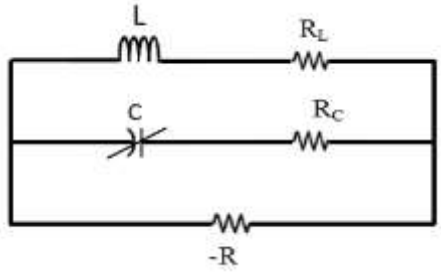


Fig. 2: LC voltage control oscillator.

Different topologies have been proposed for designing of the oscillator but the most important one is cross-coupling LC topology in RF applications. LC cross coupling topology which is proportional to the other topology has better phase noise performance. Table 1 show Comparison of ring and LC VCO based on phase noise, power and area.

TABLE I: Comparison between LC Oscillator and the Ring Oscillator.

| Ring oscillator | LC VCO |
|---|---|
| low power consumption | High power consumption |
| High phase noise | Average phase noise |
| Low area in the chip | High area in the chip |
| Integration capabilities | Integration capabilities |

This paper a cross- coupled VCO has presented that it has low phase noise and low power with using PMOS-only and switching capacitor. Further details are described section 2. The comparison and conclusion are presented in section 3 and 4, respectively.

## 2. Proposed VCO

Fig. 3 shows the schematic of the proposed VCO. Due to the low noise of PMOS, NMOS transistors are used instead of PMOS in designing VCO. In the same dimensions, PMOS transistors flicker noise is about 10 times lower than in NMOS transistors. This paper has used PMOS cross coupled VCO for reduce flicker noise in MOS devices. Also, a tail current source is employed to control the power consumption and the negative resistance. Importantly, the designed VCO exhibits low phase noise and low power due to PMOS transistor and current supply. The varactor and switching capacitor adjust oscillation frequency. The negative resistance is generated by $M_1$ and $M_2$. Negative resistance value is obtained from the following equation:

$$R_{neg} = -\frac{2}{\sqrt{C_{ox}\mu_p\left(\frac{W}{L}\right)I}} \tag{1}$$

As can be seen from Equation 1 by changing the width (W) and current supply (I) can be adjusted negative resistance. For receive oscillation, negative resistance oscillation should be less than or equal to the resistance of the parallel tank.

$$R_{neg} \leq 2R_p \tag{2}$$

Differential structure of deigned VCO reduces the power supply injected phase noise. By increasing the size of differential pair transistors ($M_1$, $M_2$), although phase noise is reduced but oscillation frequency accordingly is increased. The frequency tuning rang is required to be wide. For wide tuning rang the different, between the maximum and minimum values of capacitor would be wide. Therefore, just using varactor cannot be achieved a wide tuning rang. In this design we have used a capacitor bank to increase the frequency range. Fig. 4 illustrates the schematic of capacitor bank. When all the capacitors are connected to a frequency range of 5.65 GHz to 5.97

GHz is obtained. While none of the capacitors are connected to tank a frequency range of 6.51 GHz to 7 GHz is achieved. The oscillation frequency of the LC-tank VCO is given as:

$$\omega_0 = \frac{1}{\sqrt{L(C_{Var}+C_P+C_{bank})}} \tag{3}$$

Where $C_{Var}$ and $C_P$ are the capacitance of the varactor and parasitic capacitor respectively. The oscillation frequency is coarsely adjusted by capacitor bank ($C_{bank}$) and finely changed by varactor.

Phase noise is an important parameter to measure the performance of the oscillator. For this purpose Leeson model to calculate the phase noise is presented below [7].

$$L(\Delta f) = 10\log\left\{\left(\frac{f_0}{2Q_{tank}\Delta f}\right)^2\left[F\frac{kT}{2P_{OUT}}\left(1+\frac{f_C}{\Delta f}\right)\right]\right\} \tag{4}$$

where $f_o$ is the center frequency, $\Delta f$ is the frequency offset from $f_o$, $Q_{tank}$ is the tank loaded quality factor, $k$ is the Boltzmann constant, $T$ is the temperature, $F$ is the noise factor, and $f_c$ is the flicker noise corner frequency.

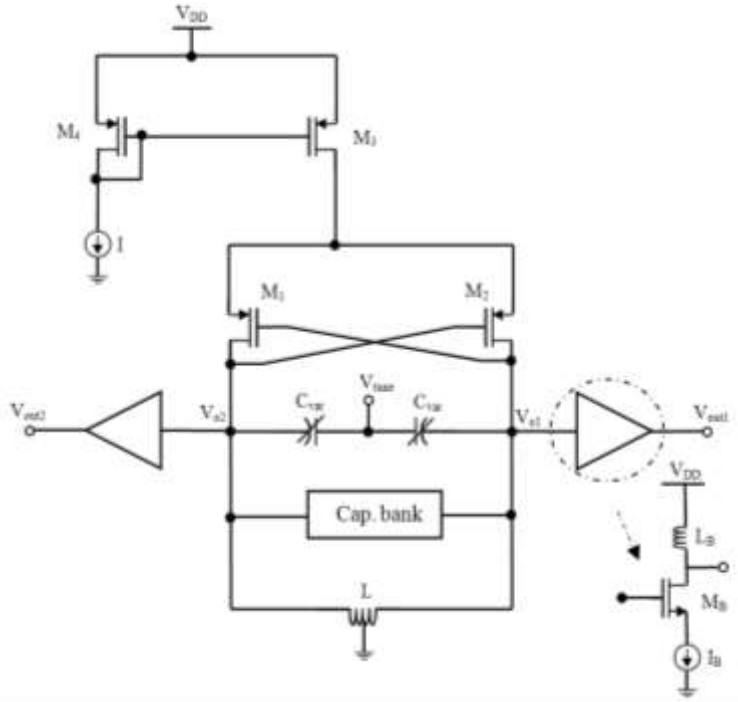


Fig. 3: Circuit diagram of designed VCO.

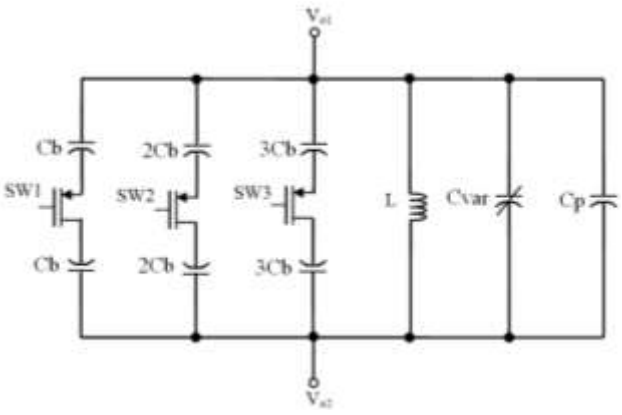


Fig. 4: The schematic of capacitor bank.

## 3. Simulation Result

The presented VCO was simulated in 0.18 µm CMOS process technology. As shown in Fig. 5, the simulated phase noise is -115.5 dBc/Hz at 1 MHz from central frequency 6.68 GHz. The output power is -12.82 dBm. Fig. 6 shown output power versus variable voltage under a supply voltage $V_{DD}$=1.2. The frequency varies with varactor and 3-bits capacitor switching. The output frequency of the designed VCO can be tuned from 5.65 GHz to 7 GHz as shown in Fig. 7. The power consumption of VCO core and buffer are 3.84 mw. To compare the performance of designed VCO with other work, a figure of merit (FOM) is illustrated as (4).The FOM of VCO is calculated -186.09 dBc/Hz [8].

$$FOM = L\{f_{offset}\} - 20\,log\left(\frac{f_0}{f_{ofset}}\right) + 10\,log\left(\frac{P_{DC}}{1mw}\right) + 20log\frac{FTR}{10} \quad (5)$$

Where $L\{f_{offset}\}$ is the VCO phase noise, $P_{DC}$ is the dc power consumption, $f_0$ is the carrier frequency. Table 2 summaries the performance of this design and compare with prior reported VCOs. The variation power supply effect the efficiency of VCO. For $V_{tune}$=0.2v and bit=000, the oscillation frequency versus power supply ($V_{DD}$) is shown in Fig. 8. VCO's phase noise performance is effected by the thermal and flicker noise of passive and active devices. Fig 9 is illustrated phase noise versus temperature when temperature sweeps from -50 to 100°c.

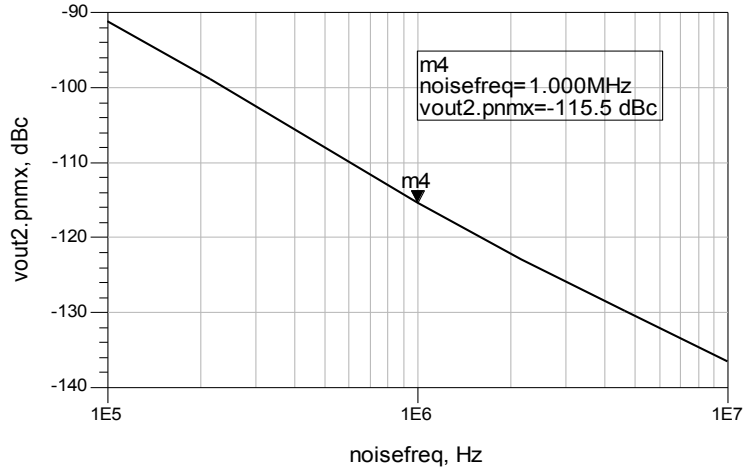


Fig. 5: The simulated VCO phase noise.

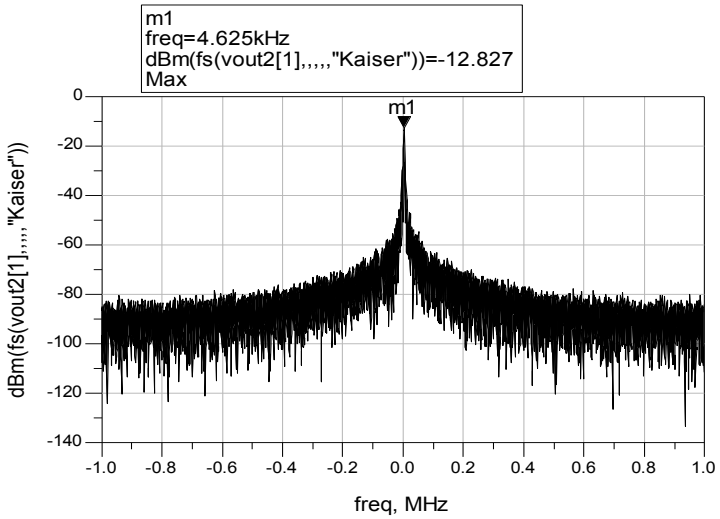


Fig. 6: The simulated output of VCO.

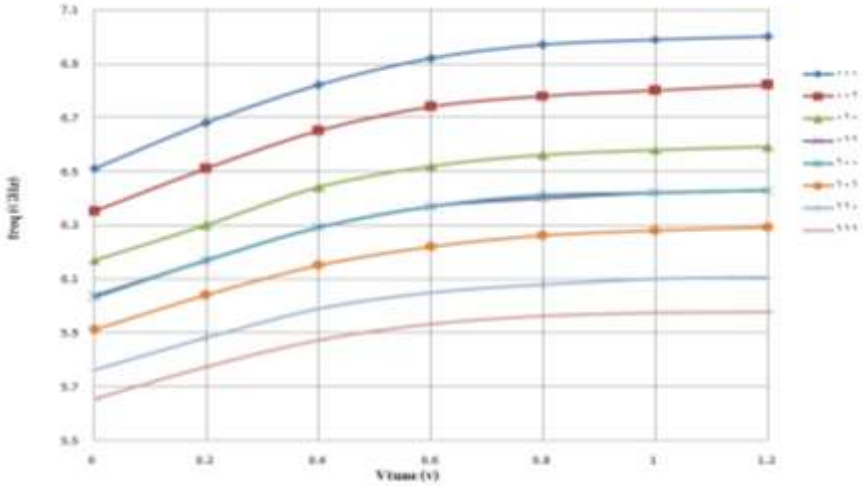

Fig. 7: Output frequency of designed CMOS VCO.

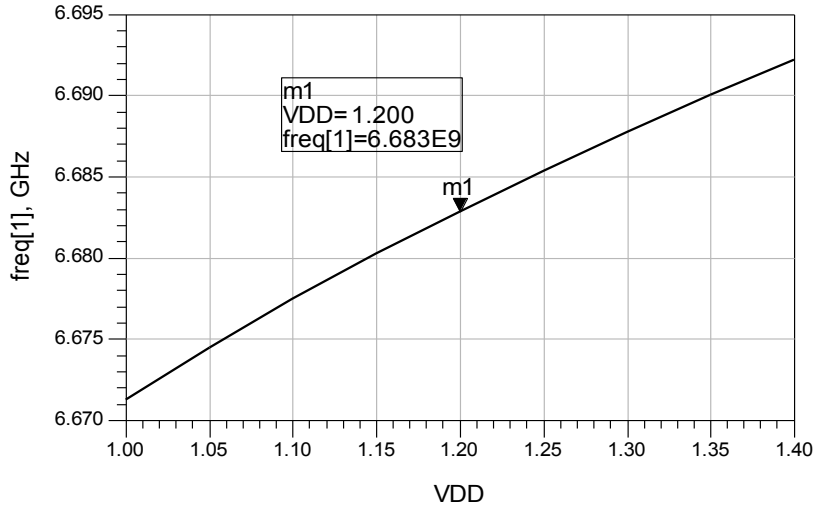


Fig. 8: Simulated oscillation frequency versus $V_{DD}$.

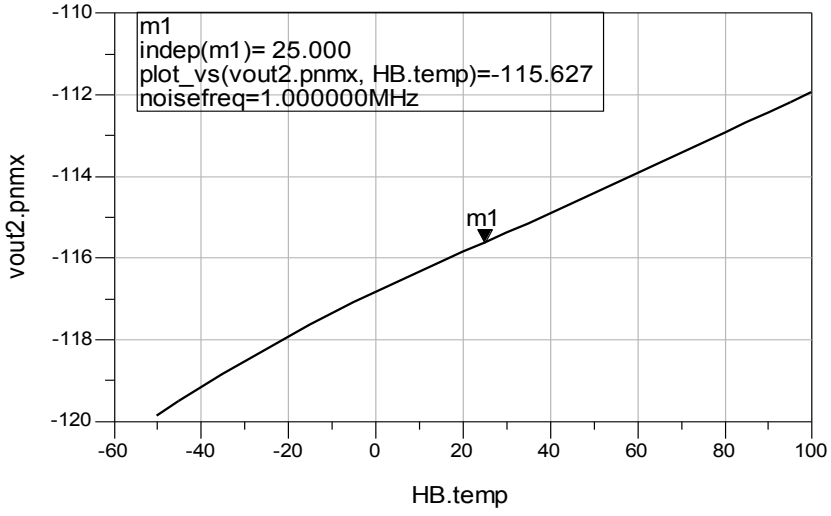


Fig. 9: Simulated phase noise versus temperature.

TABLE II: Comparison of CMOS VCOs.

| Reference | Process | $f_o$(GHz) | PN (dBc/Hz) @ offset frequency | $P_{DC}$ (mw) | FOM (dBc/Hz) |
|---|---|---|---|---|---|
| [1] | 65 nm CMOS | 3.7 | -137.1 @3MHz | 10.5 | -188.7 |
| [2] | 0.35µm BiCMOS | 5.4 | -117 @1MHz | 13.5 | -180.5 |
| [6] | 90 nm CMOS | 5.8 | -108.5 @ 1MHz | 14 | -185.1 |
| This work | 0.18 µm CMOS | 6.32 | -115.5 @1MHz | 3.84 | -186.09 |

# 4. Conclusion

A PMOS cross- coupled VCO with low phase noise and low power with wide tuning rage has been designed. Moreover, the PMOS transistors reduce flicker noise. The VCO demonstrate a phase noise -115.5 dBc/Hz at 1 MHz, a tuning range of 23.89%, and a FOM of -186.09 dBc/Hz. Also, the circuit consumes 3.84 mw with 1.2 power supply.

# 5. Reference

[1] G. Li, L. Liu, Y. Tang, and E. Afshari, "A Low-Phase-Noise Wide-Tuning-Range Oscillator Based on Resonant Mode Switching, " *IEEE J Solid-State Circuits*, vol. 47, pp. 1295 - 1308, Jun 2012.

[2] G. D. Astis, D. Cordeau, J. –M. Paillot, and L. Dascalescu, "A 5-GHz fully integrated full PMOS low-phase-noise LC VCO," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2087–2091, October 2005

[3] Q. Huang, "Phase noise to carrier ratio in LC oscillators," *IEEE Trans. Circuits Syst. I*, vol. 47, pp. 965–980, July 2000.

[4] M. Hsieh and G.E. Sobelman, "Comparison of LC and Ring VCOs for PLLs in a 90 nm Digital CMOS Process," *In Proceedings, international SOC design conference*, pp. 19-22, 2006.

[5] G. Jovanovic, M. Stojcev, and Z. Stamenkovic, "A CMOS voltage controlled ring oscillator with improved frequency stability", *Scientific Publications of the state university of NoviPazar*, vol. 2, PP. 1-9, March 2010.

[6] B. Soltanian, H. Ainspan, W. Rhee, D. Friedman, and P. R. Kinget, "An ultra-compact differentially tuned 6-GHz CMOS LC-VCO with dynamic common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1635–1641, August 2007.

[7] N. H. W. Fong, J. -O. Plouchart, N. Zamdmer, D. Liu, L. F. Wagner, and C. Plett, N. G. Tarr, "Design of Wide-Band CMOS VCO for Multiband Wireless LAN Applications, " *IEEE J. Solid-State Circuits*, vol. 38, pp. 1333–1342, July 2003.

[8] Y. Chen and K. Mouthaan, "Wideband varactorless LC VCO using a tunable negative-inductance cell," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, pp. 2609–2617, October 2010.